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***Abstract*—This paper presents an embedded measurement circuit dedicated to the extraction of the SET switching time of RRAM memory cells. A brief overview of the measurement circuit, designed in a hybrid 130nm technology with HfO_2 BEoL RRAMs, is given with emphasis on the write termination (WT) mechanism and the switching time acquisition thanks to a Time-to-Digital Converter (TDC) shift and capture mechanism. The experimental test set-up and test conditions are then described, including automated measurement script. Following our test procedure, we are able to extract the measured RRAM resistance values and the associated SET switching times, using a de-embedding process. Resistances and SET switching time values fully complies with the ones obtained in the literature through heavy waveguide measurement setups, validating our approach.**

***Keywords*—RRAM, Switching Time, Write termination, Time-to-Digital Converter**

I. INTRODUCTION

Resistive memory is currently attracting a lot of attention, due to its promising status as a versatile solution for future computing implementations. Studying the main features of this technology, such as data retention, bit-cell area, variability, and SET/RESET switching time, is of high importance to fully benefit from its potential. Most of these features can be easily extracted through probe testing memory cells or arrays. Switching time extraction, however, is not straightforward due to parasitic elements introduced by the probe testing approach. Although switching time is a critical feature in RRAMs, the results of its measurements have varied from tens of nanoseconds [1] to the sub-nanoseconds range [2], [3], when using conventional measurement tools and test structures. With advanced measurement tools and techniques, 120 ps switch time measurement [4], and even below-100 ps range, have been reached [5], [6]. These measurements require sophisticated wave-guided probe testing techniques together with dedicated test structures, in order to guarantee proper fast switching time measurement with low parasitic capacitance. These techniques are highly complex to set up and out of reach for most electronic testing labs. The precise knowledge of the switching time value is, however, mandatory at the product level to design an efficient memory controller and to embed on-chip low-power solutions such as write termination [7]. It is therefore of prime importance to propose an on-chip measurement solution to extract the switching time in a straightforward and efficient manner, close to product conditions.

In this work, we designed, manufactured, and experimentally validated, for the first time, a hybrid circuit to embed the extraction of the SET switching time of RRAM cells on-chip. The SET switch time measurement principle is based on a signal race, in a Time-to-Digital Converter (TDC), between the start of the programming signal application and the output of a Write Termination (WT) circuit. The latter stops the programming operation when the switching event is detected. The switching time is then easily acquired in an output bit-stream. The remainder of this paper is organized as follows. Section II describes the test-chip structure and how the embedded timing measurement mechanism works. Section III presents the measurement setup and details the measurements acquisition and the de-embedding process to acquire the SET switching time values together with the resistance values (Low Resistive State - LRS & High Resistive State - HRS). Section IV discusses the obtained resistance and timing results and validates our approach regarding state-of-the-art values.

II. TEST STRUCTURE

The presented solution is composed of three main blocks: a memory array, a write termination circuit (Fig. 1), and two Time-to-digital converters (Fig. 2), one for the SET and one for the RESET. The memory array is composed of a row of sixty-three 1T1R RRAM cells and one 1T cell without RRAM. The 1T cell is used for timing and resistance overhead de-embedding. All the 64 cells of the array are connected to common shared Source and Bit lines as presented in Fig. 1. The selection of the cell to be measured is performed through a shift register (not represented in Fig. 1), that connects the word line to the selected cell gate. The gates of unselected cells in the array are all grounded. As depicted in Fig. 1, a write termination circuit [7] is connected to the memory array to detect the switching event. The SET operation starts by setting the EN_{SET} signal to V_{DD}, to connect the bit line to the input voltage V_{SET} through transistor M1. The source line is grounded through transistor M6. When a SET event occurs, the flowing current in the selected memory cell rises to the

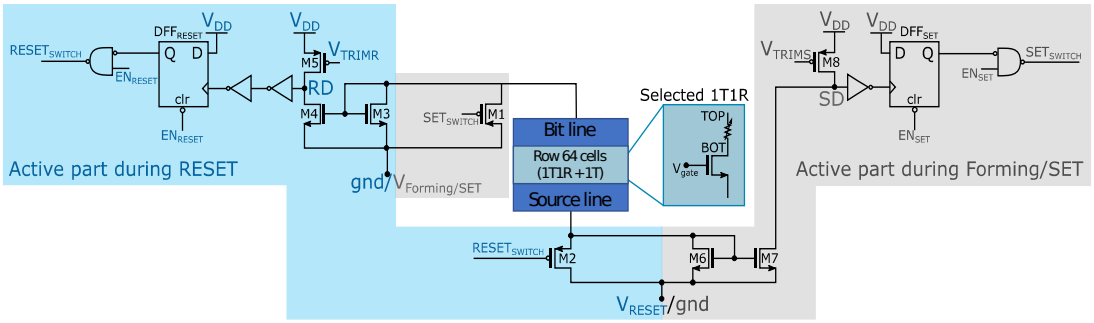

Fig. 1. Write termination (WT) circuit schematic, including the row of 64 cells (63 1T1R cells and one 1T cell without RRAM) to be characterized. The shift register used to connect the gate of the selected cell to the word line is not represented. Bit-line and Source-line are shared between all cells in the row.

compliance current set by the word line voltage. The copy of the current ensured by the transistor M7 generates a rising edge on the input clock of DFF_{SET} that inhibits the signal SET_{SWITCH}. As the latter signal rises to V_{DD}, M1 is turned off, and the SET operation is terminated. The Time-to-Digital Converter, depicted in Fig. 2.a. acquires the operation time during the full SET process.

The TDC is designed with 400 identical elements. Each TDC element is composed of a NOR gate that takes as input the SET_{SWITCH} and the delayed ENb_{SET}, thanks to a 50ps propagation time buffer. The NOR gate output is connected to the clock input of a rising edge D-flip-flops. Before starting the measurement process, we reset all the TDC D-flip-flops to make sure that all the outputs are zeros. As we raise the EN_{SET} signal to V_{DD}, ENb_{SET} falls to zero, the measurement process starts, and the chain of flip-flops start to capture ones with the propagation of rising edge on the D-flip-flops clock input, following the propagation of ENb_{SET} through the delay chain. When a switching event occurs, the SET_{SWITCH} signal rises and hence terminates the SET operation and simultaneously the capture process in the TDC. Indeed all the NOR gates outputs are then set to zero, inhibiting falling edge on the TDC D-flip-flops clock input, as schematically reported in Fig. 2.b.

At the end of the measurement phase, the number of ones captured in the TDC represents an image of the operation time during the full SET process. Thus, this time includes the switching time and also the write termination circuit response time. The TDC bit-stream is then duplicated in an output shift register to shift out serially the operation time. As the buffer propagation delay is 50ps, the measurement uncertainty on the operation time is theoretically $\pm$ 50ps.

The proposed structure is designed in a hybrid 130nm CMOS process with HfO_2 RRAM processed between metal layers four and five. The circuit layout is reported in Fig. 3.a covering an area of 1900×560 μm^2 including the access PADs. Fig. 3 presents the optical microscopy photograph of the chip in (b) and an SEM image (c) of the RRAM memory stack on top of the CMOS process.

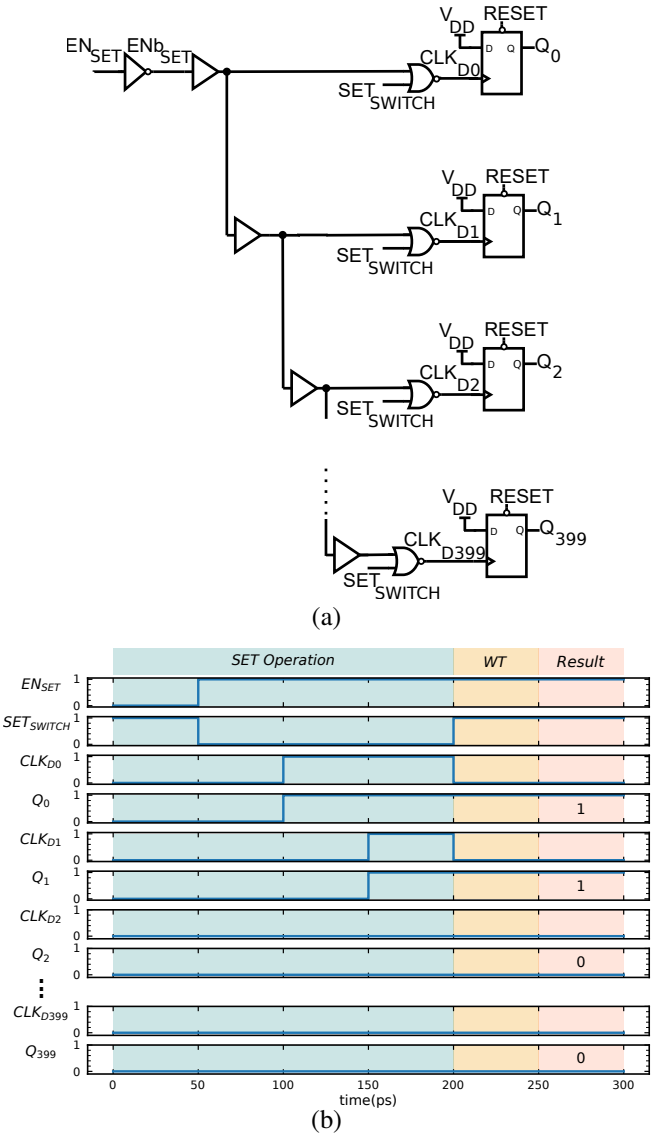

Fig. 2. Time to Digital Converter (TDC) circuit schematic (a) and functionality scheme (b). After measurement the number of '1' in the bit stream gives the time between the start of SET operation and the detection of a switching event with the WT circuit

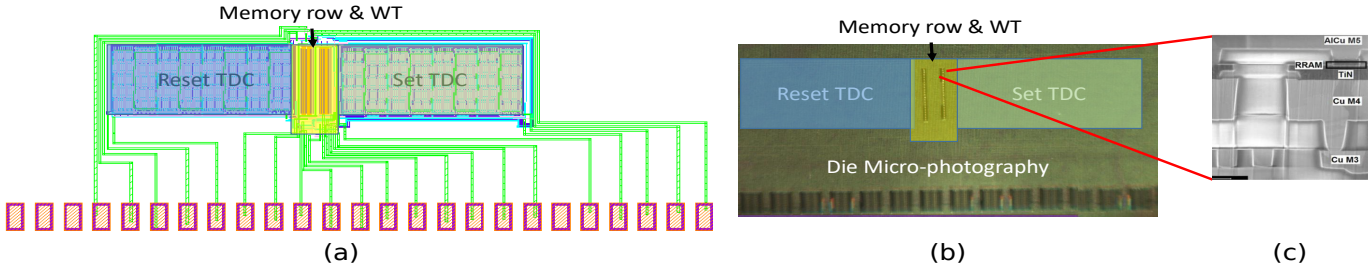

Fig. 3. (a) Layout, (b) die optical microscopy photograph of the measurement structure, with identification of the functional blocks, and (c) SEM image of the memory stack on top of the CMOS process

Measurement conditions	value
V_{SET}(V)	2.1 to 2.7
V_{RESET}(V)	3
V_{FORM}(V)	2.9
$V_{GateSET}$(V)	2.5 to 2.9
$V_{GateRESET}$(V)	5
$V_{GateFORM}$(V)	2.9
V_{TRIMS}(V)	0.45 to 0.52
SET time(noWT)(ns)	10
RESET time(ns)	10

TABLE I
VOLTAGE AND TIMING CONDITIONS USED DURING THE MEASUREMENT TO FORM, SET, AND RESET THE MEMORY CELL.

III. MEASUREMENT SETUP AND DE-EMBEDDING PROCESS

The chip is directly measured on wafer using a 25-pad probe card mounted on a 200mm probe station. The digital control signals are generated with an STMicroelectronics STM32 microcontroller unit. These signals are not directly connected to the probing card due to the potential difference between the STM32 output voltage and the die digital input voltage. Thus, a level shifting PCB is used to adapt voltage values between the microcontroller unit and the chip. In addition, to control digital signals, the STM32 also captures the digital outputs of the chip and ensures communication with the computer. The analog signals V_{SET}/V_{FORM}, V_{RESET}, EN_{SET} and EN_{RESET} are provided by a Keysight B1500A Remote Sense Units to be able to measure current values during operations and resistances (LRS & HRS), after each SET or RESET operations. Whereas the other signals, either analog or power supply, are provided by a DC stabilized Power supply. All the applied voltages for analog signals are given in Tab. I. To automate the measurement, a python script is used Fig. 4. The script's goal is to communicate with all the signal generators, STM32 microcontroller, the power sources, and to capture and save all the measured resistance values and the SET operating time values. These measured values are then post-processed with de-embedding python scripts.

The first step of the measurement procedure is to select the cell under test from the sixty-three 1T1R cells. Then we configure the voltage levels used for forming operation and we launch the Forming process. The program checks if the forming operation is successful or not based on measured current values. After forming the operation, a 200 SET/RESET

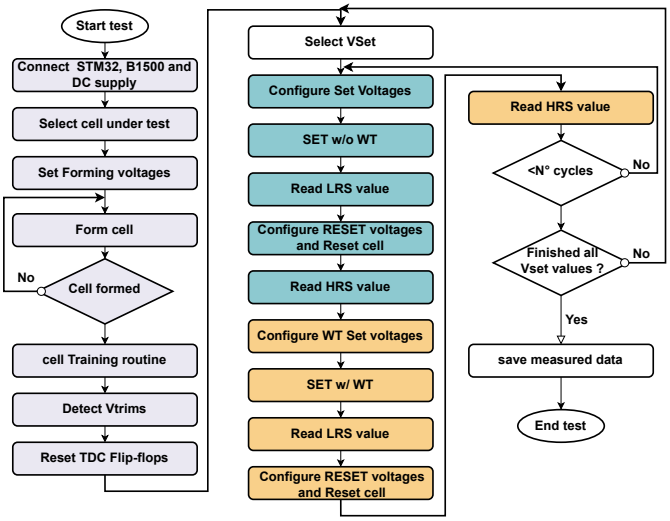

Fig. 4. Flowchart of the python script used to automate the measurements

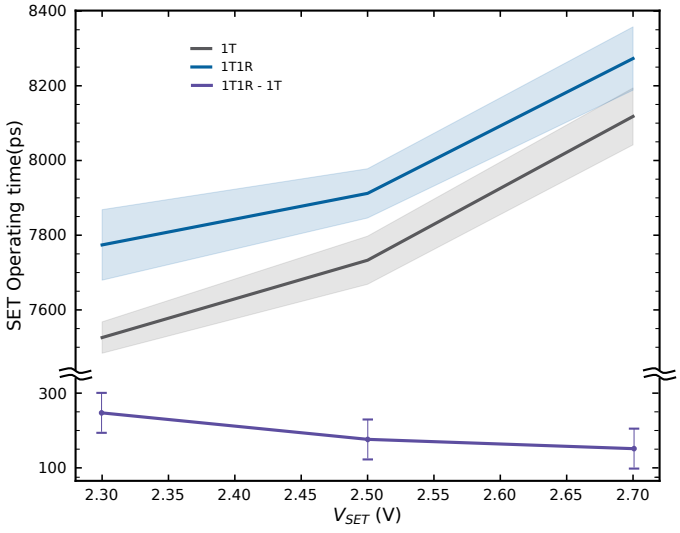

Fig. 5. Mean switching time measurement including WT response time for 1T and 1T1R configuration for $V_{GateSET} = 2.7V$, with measured uncertainty. Results are established with 8000 cycles on a single cell

routine is launched to wake up the selected memory cell. This wake-up routine is performed to stabilize the LRS and HRS values to the target values. After this routine, we launch

a series of SET with WT to detect the minimum V_{TRIMS} value to trigger the write termination for the lowest V_{SET} value. Then, we start the resistance and timing extraction process. At first, we reset all the flip-flops of the SET TDC block using the STM32. Then, we select a V_{SET} value, and we set up all the voltages on the DC power supply and the Keysight B1500A. The first phase in this process is a conventional SET, without write termination (noted SET w/o WT), followed by a RESET operation. After each operation, we apply a reading voltage on the selected 1T1R bit-cell through transistors M1 and M6 using the Keysight B1500A. During this phase, we extract the resistance value with the current measurement. The same measurement is conducted on the 1T cell. After these measurements, we repeat the same operation with write termination enabled (noted SET w/ WT), with the extracted V_{TRIMS} value, on both the 1T1R selected cell and the 1T cell. Here also, a read procedure is performed to extract the resistance values. Since the WT is enabled, timing measurement is also performed and the STM32 acquires the timing measurements. This extraction process is repeated for different V_{SET} values and a predefined number of cycles.

After completing the testing phase, the raw measured resistance and SET operating time values are processed. The de-embedding is based on the difference between the measured values obtained on the 1T cell and the selected 1T1R cell. By subtracting the impedance of the 1T cell from the impedance of the 1T1R configuration, we can remove the contributions of the select transistor, and transistors M1, M6. Doing so, we extract the RRAM LRS and HRS values. Similarly, by subtracting the output bit-stream of the TDC for the 1T cell from the one of the 1T1R, we can remove all the circuit delays, including WT response time, and thus extract the RRAM SET switching time.

The Fig. 5 illustrates the SET operation time raw measurements performed on 1T and 1T1R cells. Mean values and measurement dispersion are plotted for different V_{SET} voltages, for 8000 cycles on a single cell. One can observe a similar trend for the circuit response time with 1T and 1T1R configurations. Thus, the difference between both measurements represents clearly the RRAM SET switching time and can be extracted by subtracting both curves.

IV. Results and Discussion

Using the proposed embedded measurement solution, it is possible to extract HRS and LRS values, with and without write termination, in a very straightforward manner. Fig. 6 presents both types of distributions, i.e. the LRS distribution without termination (SET w/o WT), the LRS distribution with termination (SET w/ WT), and the HRS distribution without termination after both types of SET (w/ and w/o WT). First of all, it appears that the activation of the write termination during the SET process does not influence the subsequent RESET operation, since the two HRS distributions perfectly overlap. Knowing that the write termination is not activated during the RESET and the RESET process is self-limiting, it appears

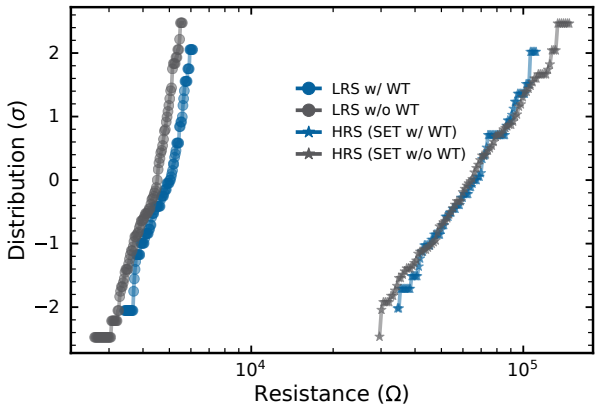

Fig. 6. HRS and LRS values with (blue) and without WT (gray) after de-embedding process for $V_{TRIMS} = 0.45V$, $V_{GateSET} = 2.9V$ and $V_{SET} = 2.7V$.Results are established with 8000 cycles on a single cell

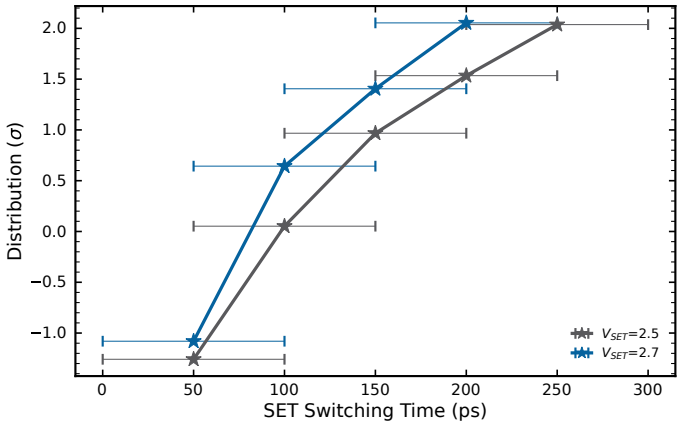

Fig. 7. RRAM SET switching time after de-embedding process for two different V_{SET} conditions with $V_{GateSet} = 2.9V$ and $V_{TRIMS} = 0.45V$. Results are established with 8000 cycles on a single cell

that the RESET time is sufficient to break the conductive filament, whatever the previous SET operation type (w/ or w/o WT). Second, the write termination has a strong influence on the LRS values. Indeed the LRS distribution with write termination exhibits higher values than the one without write termination. Since the cell without termination is stressed after the switching event, this leads to a stronger conductive filament creation and thus a lower LRS value [8].

Our embedded SET switch time measurement solution allows fast and simple timing extraction. Thus, it is possible to extract SET switching time distributions on-chip, using the de-embedding procedure presented in the section III. The Fig. 7 presents the switching time distributions obtained from 8000 measurements on a single cell, with two different V_{SET} (2.5V and 2.7V), for fixed $V_{GateSET}$=2.9V and V_{TRIMS}=0.45V. First of all, please note, that the switching time unit and the measurement uncertainty of $\pm$ 50ps, are linked to the TDC delay chain design. The measured SET switching time ranges from 50ps to 250ps. Moreover, a slight dependency of the

SET switching time with the applied SET voltage is also noted. This behavior is a well-known effect of the RRAM. Indeed, it has been already demonstrated on a larger time scale (ns to ms) that the SET switching time decreases when the applied SET voltage increases. Finally, the SET switching times measured with our embedded structure agree with the ones measured with wave-guide direct measurements [4]–[6], which fully validates our test structure.

V. Conclusion

In this work, we proposed for the first time an embedded measurement solution to capture RRAM SET switching time, together with LRS and HRS values. The proposed solution is based on a Write Termination block associated with a TDC, to capture the switching time as a bit-stream. This circuit is close to a product context and offers the capacity to extract switching measurements on a large cells population. The circuit is tested on a probe station with a microcontroller unit to manage control signals and Keysight B1500A and DC stabilized power supplies to provide the analog signals and power supply. A de-embedding solution, based on measurements subtraction between 1T1R and 1T cell is proposed. Finally, we show that the WT process has an impact on LRS distribution. We achieve SET switching time measurement from 50ps to 250ps, which is in line with the state-of-the-art values obtained with heavy wave-guide measurement. This fully validated our solution.

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